REMARKS

Claims 1-11 are pending in the application. All claims were rejected. An Advisory Action has been received, in which the Examiner indicated that claim amendments were not entered, and that the references to specific passages in the specification, made using paragraph numbers, could not be understood.

With regard to the claims, the response filed on January 6, 2004 clearly and conspicuously notes that the claims were NOT amended, and thus all were listed as "previously presented." The claims listed in that response were intended to be and believed to be an accurate reproduction of the current state of the claims, as amended on July 22, 2003. On careful review, it appears that in Claim 7, the phrase "the splitting means" was included although it was not actually inserted in the July 22, 2003 amendment (despite being intended and believed to have been added at that point). In all other respects, the January 6, 2004 listing of claims appears to be correct. The undersigned apologizes for this error; the claims as amended on July 22, 2003 were the correct claims, and no amendment was intended on January 6, 2004. Claim 7 has now been amended to add this phrase.

Claims 1, 7, 8, and 11 have been amended. Claims 7 and 8 are amended to place them in independent form, and claim 7 includes the phrase "the splitting means." Claims 1 and 11 have been amended to specifically include a characteristic of the all-pass splitting means as described in the specification. The scope of claim 8 has not changed at all.

With regard to the various specific references to the specification, a table of the paragraph numbers, as referenced in the previously-filed response, and the corresponding page/line numbers is below. Also, for the Examiner's convenience, a copy of the published patent application is attached, which includes paragraph numbers. The undersigned had assumed

such was available to the Examiner.

Paragraph Number	Specification Page/Line Numbers
0030	Page 6, lines 1-2.
0031	Page 6, lines 3-4.
0036	Page 6, lines 15-20.
0048	Page 8, line 10-18.

35 U.S.C. § 112(1) – Enablement

Claims 7-8 were rejected as non-enabled by the specification. The Examiner reads the limitations of these claims as shown in Figures 5 and 6, each described in paragraphs 0030 (page 6, lines 1-2) and 0031 (page 6, lines 3-4), respectively, as an "all-pass network," as implementations of the "all-pass circuit" element 10 of Figure 4 is described.

Claims 7 and 8 describe different structural implementations of the "splitting means" of Claim 1, and have been amended into independent form.

Figure 4 depicts a quadrature phase shifter including a transimpedance amplifier 12 performing voltage-to-current conversion and generating a current iin fed to all-pass circuit 10. Equation (6) defines the transfer function for an idealized all-pass circuit 10. As depicted in Fig. 4 and reflected in equations (8), all-pass circuit 10 receives iin and produces i1, which is phase-shifted by 0° (i.e., not phase-shifted at all), and i2, which is phase-shifted by 90° (note that the term for i2 in the center of equations (8) is the input current iin multiplied by the idealized transfer function from equation (6)).

Figure 5 shows input signal i_i, which is mirrored to phase-shifted output i_o. The skilled artisan recognizes that Figure 5's i_i corresponds to Figure 4's iin, and Figure 5's i_i and i_o correspond to Figure 4's i1 and i2, respectively. The transfer function of the circuit of Figure 5 is $\frac{i_o}{i_i} = \frac{sC/g_m - 1}{sC/g_m + 1}$, so that the time constant can be tuned by adjusting I_{BIAS}.

Figure 5 is a single-ended implementation of a phase-shifter within all-pass circuit 10, for phase-shifting current i2. Of course, all-pass circuit 10 includes other portions (at a minimum, a splitting function to produce currents i1 and i2 based on iin). Note that equation (9) for I_o/I_i matches the idealized transfer function of equation (6). From this correspondence in transfer functions, those skilled in the art will recognize that i_i in Fig. 5 is taken from iin in Fig. 4 and i_o is output as i2 (recall that signal currents are indicated in lowercase, such as i_i, while total currents including any DC component are indicated in uppercase, such as I_i). Fig. 5 thus depicts the phase-shifting portion of all-pass circuit 10 used to phase-shift current i2 relative to input current iin, while current i1 is passed through all-pass circuit 10 without phase-shifting.

With regard to Figure 6, applicant first notes that the application specifically describes that the inputs to the circuit can be either voltages or currents (see, e.g., paragraph 0036 on page 6, lines 15-20), and Claim 1 does not specifically require either, so the Examiner's observation that the circuit of Figure 6 receives input voltages does not appear to be relevant. Paragraph 0048 (page 8, lines 10-18) describes that the input voltage is converted into current, and following paragraphs describe this circuit as producing current i_A and corresponding phase-shifted current i_B at the output.

Fig. 6 is a differential implementation of a phase-shifter within all-pass circuit 10, but also includes the transimpedance amplifier 12 performing voltage-to-current conversion of the

input voltage across IN+ and IN- to currents I_A and I_B. Specification, page 8, lines 10-13. Note that equation (11) for I_B matches the bottom of equations (8) (for i1-i2), while equation (10) for I_A is simply the top of equations (8) (for i1+i2) multiplied by -1. As depicted in Fig. 6, currents I_A and I_B are used to produce in-phase differential output current I and quadrature-phase differential output current Q, corresponding to currents i1 and i2 in Fig. 4.

Note that an important characteristic of all-pass circuit 10 is that the phase-shifting, whether implemented in a single-ended or differential fashion, is controlled by transconductance g_m (and capacitance C) rather than a resistance R (and capacitance C) as in the prior art embodiment of Fig. 2.

One of skill in the art understands that the circuits shown in both Figures 5 and 6 receive an input signal and produce corresponding phase-shifted output signals, as does element 10 in Figure 4.

Figures 5 and 6, and claims 7 and 8, are therefore believed to be fully enabled, and these rejections are traversed.

35 U.S.C. § 112(2) – Definiteness

Claim 7, as currently amended, and claim 8, as previously amended, both specifically apply to the splitting means of claim 1. Claims 7 and 8 both clearly and distinctly describe the circuit structure of the splitting means, and one of skill in the art would clearly understand what the applicant claims as his invention.

Claims 7 and 8 specify the structure of alternate embodiments of the "splitting means," and it is believed that the structure described is sufficient to particularly point out and distinctly claim the particular structures. Indeed, it is hard to imagine that one of skill in the art would not

immediately understand the interrelation of all elements described in each of these claims. The interrelation of the splitting means and the other elements of these claims is also clear.

All §112(2) rejections are traversed. However, if the Examiner has a specific concern or suggestion as to how these claims may be made even more clear, he is respectfully invited to telephone the undersigned attorney.

35 U.S.C. § 102 – Anticipation

Claims 1-6 and 11 have been rejected as anticipated by Ishihara (USP 6,054,883). The Examiner correctly notes that some elements of Ishihara appear to be similar to elements of claim 1. Claim 1 and 11 have been amended to specifically require that the splitting means also have the characteristics of an "all-pass," and a time constant of C/g_m, as described in paragraph 42: on page 7, line 11 of the specification as filed.

Nothing in Ishihara appears to teach or suggest this feature. Ishihara discloses a phase shifter PS1, but does not disclose or discuss whether this phase shifter acts as an all-pass or not. Certainly, as phase shifter PS1 is a known RC-CR shifter, its time constant is not defined by its transconductance, as in Claims 1 and 11.

As an anticipation reference must teach EVERY aspect of the claims, and Ishihara does not, Ishihara fails to anticipate claims 1-6 and 11.

The anticipation rejections are traversed.

35 U.S.C. § 103(a) – Obviousness

Claims 7, 9, and 10 were rejected as obvious over Ishihara in view if Liu (USP 6,496,545). Applicant notes that no proper motivation to combine the Ishihara and Liu

references has been stated. While both Ishihara and Liu incorporate phase shifters, Liu is directed toward a side-band mixer, and there is no indication that one designing a phase shifter, or even a phase shifter with error detection, would look to a side-band mixer patent for any teachings, nor that Ishihara is at all concerned with sideband rejection.

Moreover, although Liu's Figure 5A does indeed include two transistors and a capacitor, they are not connected to each other (or to themselves) as described in claim 7. As such, even this combination of references fails to meet the claim limitations.

Therefore, a *prima facie* obviousness rejection has not been made, and all obviousness rejections are traversed.

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SUMMARY

All claims are believed to be in condition for allowance. If the Examiner has any further suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@davismunck.com***.

The Commissioner is hereby authorized to charge $86.00 for the additional claim filing fee, as well as any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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